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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,926	03/30/2001	Giovanni Campardo	856063.689	7548

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SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVE
SUITE 6300
SEATTLE, WA 98104-7092

EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,926	CAMPARDO ET AL.	
	Examiner	Art Unit	
	Guy J. Lamarre	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2005* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 2-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 2-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *9 Jan. 2004* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. This office action is in response to Applicants' amendment of 14 February 2005.

1.1 **Claims 2-22** remain pending in response to Applicants' election with traverse.

1.2 The prior art rejections of record are maintained in response to Applicants' amendment.

1.3 The objections and rejections under **35 USC § 112 SECOND PARAGRAPH** of record are withdrawn in response to Applicants' amendment.

Response to Arguments

2. Applicants' arguments jointly re: the prior art of record have been fully considered but are not deemed persuasive because Applicants'admitted prior art, at paras. 2-13, especially at para. 13, discloses equivalent means for external data/testing device to impose data/test vectors to device under test and sequencing operations (read/write/erase, program, simulate) means, said device made of logic and memory for verification purposes.

Claim Rejections - 35 USC ' 103

3.1 **Claims 2-5, 6-8** and **16-18, 19-21, 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Mullarkey** et al. (US 5,732,033) in view of **Bond et al.** (US 4,450,559) in further view of **Russ et al.** 'Non-intrusive built-in self-test for FPGA and MCM applications;'IEEE; page(s): 480 – 485; 8-10 Aug. 1995.

Referring to **claims 2-5, 6-8, 16-18, 19-21** and 22, **Mullarkey** teaches to use "an integrated memory device 10" (see Fig.1) comprising "a memory array 12", including "a plurality of memory cells 22", "control circuit 16", and "a test mode 20" provided for operating the memory device 10 i n a test regime.

Mullarkey does not explicitly point out to use two memories, but **Bond et al.** teaches to comprise two memories- "main memory system 11" and "secondary memory unit 13" (see Fig.1) coupled with the "electronic control system (ECC) 10". **Bond et al.** does not explicitly point out that both of memories are internal, inherently teaching for any combinations (internal/external)

of two memories. Also, it is well known that mostly integrated circuits do not contain the test operation memory (accept some specific integrated circuit particularly intended, e.g. for memory testing).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify **Mullarkey** with the teaching of Bond by simply using one memory as internal and second memory as external, because one of ordinary skill in the art would simply use an external memory for the test of the memory into integrated circuit to provide minimization of the integrated circuit (IC) dimensions, universality of application, and convenience for the test equipment.

While Mullarkey and **Bond et al.** substantially disclose the procedure for the claimed means, **Mullarkey** and **Bond et al. fail to specifically mention** the external test operation means for testing the DUT.

However such approach of is well known, especially since off-line testing is often required.. For example, **Russ et al.,** in an analogous art, discloses BIST algorithms for FPGA and MCM applications, wherein such techniques are described. {See **Russ et al.,** Id., Abstract and Introduction, and Fig. 2.}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Mullarkey** and **Bond et al.** by including therein external test operation means as taught by **Russ et al.,** because such modification would provide the procedure disclosed in **Mullarkey** and **Bond et al.** with a technique whereby it is possible to design a BIST system "*the normal system function can be reprogrammed during off-line testing to provide BIST capabilities for testing external devices... connected to the FPGA such that no area or performance penalties are incurred by the system function.* " {See **Russ et al.,** Id., page 480 penultimate para., at col. 2. }

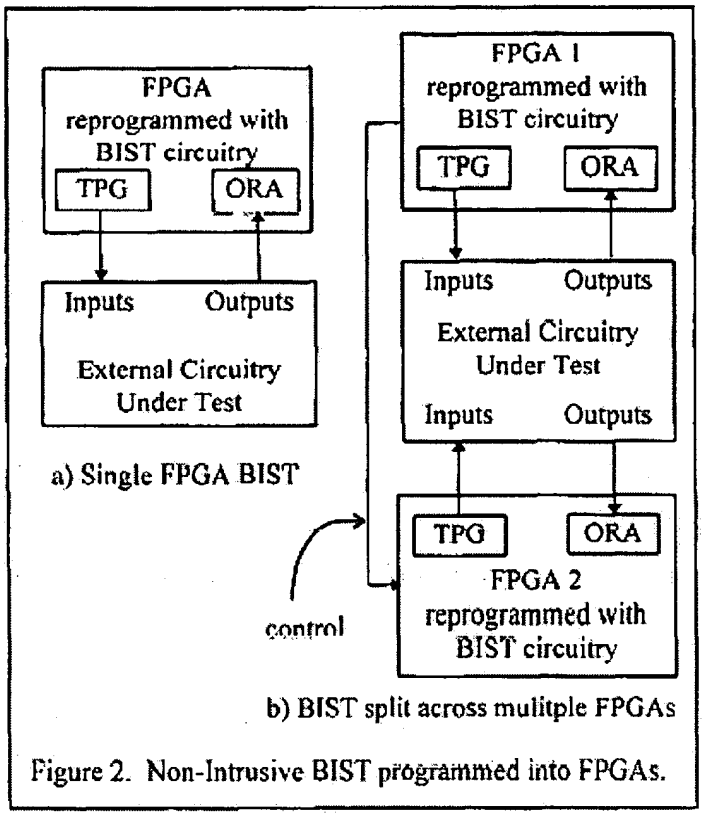

Figure 2. Non-Intrusive BIST programmed into FPGAs.

Claims 7, 8 depend from respective claim 6, hence inherit the rejection in claim 6. Also, according to claim 7, Mullarkey teaches to use the "input/output circuits 18" (column 3, lines 41, 42) and contacts (e.g. "contact 99" /see column 8, line 32, and Fig.6/) for connections. Additionally, it is well known that the integrated circuits and/or electrical/electronic devices are provided with data pins and/or address pins for connection of the integrated circuit (IC) and/or electrical/electronic devices, and explicitly pointed out and disclosed, for instance, in device by Mullarkey.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify or simply, to use Mullarkey's input/output circuit and/or contacts for connection, because one of ordinary skill in the art with the teaching of Mullarkey by including use the contacts (pins) for electrical connection of the external electronic

components, because (IC) are obviously needed to be electrically connected to the PCB (Printed Circuit Board) and/or test equipment, that can be provided the use of pins and/or contacts.

3.2 **Claims 8-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Mullarkey et al. (US 5,732,033) in view of **Russ et al.** 'Non-intrusive built-in self-test for FPGA and MCM applications;'IEEE; page(s): 480 – 485; 8-10 Aug. 1995 in further view of Kumakura et al. (US 5,566,386).

Applicant claims the nonvolatile type of the external memory unit 7. Mullarkey does not explicitly teach and point out to nonvolatile memory, inherently teaching to use any kind of memory, but Kumakura et al. teaches to use "a nonvolatile semiconductor memory and a test method for the same" (e.g. , see a title and cross specification) and Applicant admits that such is well known in page 1 line 6.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Mullarkey and **Russ et al.** with the teaching of Kumakura by using inherently any kind of memory for testing, including the nonvolatile memory, because the memory test equipment, providing the test of the memory and control logic operability, mostly (by their purpose and application) is developed as an universal device for testing of the different kinds of integrated memory circuits, logically including the nonvolatile memory.

Referring to claim 9, the device by Mullarkey et al. Includes the "memory array 12", "control means 16" and "test mode 20" (column 3, lines 40-43), Mullarkey does not explicitly teach and point out to the external test control, but teaches to use a control circuit 16, a test mode 20 and appropriate memory array (inherently internal) 12, including a plurality of "memory cells 22" (column 3, line 49), provided for operating the memory device 10 in a test regime.

Kumakura at el. teaches the test control means including "operation logic circuit 3", "command register 2" (column 6, lines 61, 62), "test cell 19", "switching circuit 7" (column 6,

line 64), "timing generating circuit 10", "erasure source control circuit 18" (column 7, line 8), and other analogous means presented in the applicant's claims. Also, it is well known that some integrated circuits do not contain the test control device (except for specific integrated circuit particularly intended, e.g. for memory testing devices).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Mullarkey with the teaching of Kumakura by using the test control device as a testing equipment, because mostly the test control devices are external apparatus, and it is well known and obvious, that test control devices can include the circuit for simulating the internal memory array in order to provide maximally efficient test of the internal memory operability. Simulation allows for system operation observation prior to commitment to hardware so as to save costs.

Claims 10, 11 depend from respective claim 9 hence inherit the rejection in claim 9.

Also, claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mullarkey et al. (US 5,732,033) in further view of **Russ et al.** 'Non-intrusive built-in self-test for FPGA and MCM applications;'IEEE; page(s): 480 – 485; 8-10 Aug. 1995.

Mullarkey teaches to use the input/output circuits 18 (column 3, lines 40, 41) and contacts (e.g. contact 99 /see column 8, line 32 and Fig.6/) for connections. Additionally, it is well known that the integrated circuits and/or electrical/electronic devices can be provided with the contacts or connector for detachable connection, for instance, by a socket. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify or simply to use Mullarkey's input/output circuit and/or contacts/connectors for connection, because one of ordinary skill in the art with the teaching of Mullarkey by including use the detachable connection (e.g. connector) for electrical connection of the external electronic components (e.g. semiconductor substrate) to, for example, PCB and/or test control unit in order

to provide sufficient universality of the test equipment. **Russ et al.** teaches to use the input/output circuits in, e.g., Fig. 2.

3.3 Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mullarkey et al. (US 5,732,033) in view of **Russ et al.** 'Non-intrusive built-in self-test for FPGA and MCM applications;'IEEE; page(s): 480 – 485; 8-10 Aug. 1995 in further view of Kumakura et al. (US 5,566,386).

Mullarkey et al. teaches, that the memory device comprises the circuit for simulating the memory array and the circuit for simulating the control logic circuit integrated into test device ("invention provides an arrangement for rapidly equilibrating the paired digit lines of the memory array of a semiconductor memory device, such as a dynamic random access memory device", e.g., see column 9, lines 20-24), during testing of the memory device. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify or simply to use Mullarkey's integrated means, because one of ordinary skill in the art with the teaching of Mullarkey by including circuit for simulating the internal memory array and the circuit for simulating the control logic circuit into test device, that is mostly the regular procedure for internal memory array test providing the efficient memory test result.
Referring claims 12, 13, Mullarkey et al. teaches, that the memory device comprises the circuit for simulating the memory array. Mullarkey et al. does not limit and/or explicitly point out the memory array location, inherently teaching to use any and all possible locations of the memory array.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify or simply to use Mullarkey's memory array, for example, as an external, because one of ordinary skill in the art with the teaching of Mullarkey by including circuit for simulating the internal memory array into test device, that is mostly the regular

procedure for internal memory array test providing the efficient memory test result by external memory array, located into the test equipment.

3.4 Claims 14, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mullarkey et al. (US 5,732,033) in view of **Russ et al.** 'Non-intrusive built-in self-test for FPGA and MCM applications;'IEEE; page(s): 480 – 485; 8-10 Aug. 1995 in further view of Kumakura et al. (US 5,566,386).

According to claim 14, Kumakura et al. teaches to operate (simulate) the test control means including "operation logic circuit 3"', "command register 2" " (column 6, lines 61, 62), "test cell 19", "switching circuit 7" (column 6, line 64), "timing generating circuit 9", "erasure source control circuit 18" " (column 7, line 8), and other analogous means presented in the applicant's claims.

Kumakura does not explicitly teach and point out to the external location of any or some means, inherently teaching to use a control circuit 16, a test mode 20 and appropriate memory array (inherently internal) 12, including a plurality of memory cells 22, for operating the memory device 10 in a test regime.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kumakura with the teaching of by using the external location of any/some means for memory test, because it is obvious and well known, that the procedure for most tests and particularly for memory test control apparatus includes steps of simulating the circuits, performing the test, and observing interactions and results, considering the purpose of the testing equipment.

Referring to claim 15, Kumakura et al. teaches to operate (simulate) the test control means including "operation logic circuit 3", "command register 2", "test cell 19", "switching circuit 7", "timing generating circuit 9", "erasure source control circuit 18", and other analogous means presented in the applicant's claims. Kumakura does not explicitly teach and point out to

the external location of any or some means, inherently teaching to use a "control circuit 16", "a test mode 20" and appropriate "memory array (inherently internal) 12", including a plurality of "memory cells 22", for the memory device 10 in a test regime.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kumakura with the teaching of by using the external location of any/some means for memory test, because it is well known and follows from the IC technology ideology, that in order to increase degree of IC's integration and universality they do not include the test circuits (except some specific IC), and obviously such means for memory test have to be externally located into test apparatus

3.5 Claims 1-5 are similar to claims 6-15, and are rejected based on the same rationale thereof.

Conclusion

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Hand-delivered responses should be brought to Customer Services, 220 20th Street S., Crystal Plaza II, Lobby, Room 1B03, Arlington, VA 22202.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
6/13/2005